University of Mumbai

687

FIRST HALF 2015

EXAMINATION TIME TABLE
PROGRAMME - M.E. (ELECTRONICS ENGG.)
SEMESTER - II

Days and Dates	Time	Paper
Wednesday, May 13, 2015	11:00 a.m. to 02:00 p.m.	Microprocessor and Systems – II.
Tuesday, May 19, 2015	11:00 a.m. to 02:00 p.m.	VLSI Design.
Monday, May 25, 2015	11:00 a.m. to 03:00 p.m.	Elective III/IV – Power Electronics.
Friday, May 29, 2015	11:00 a.m. to 03:00 p.m.	Elective III/IV – Modern Digital Signal Processing.
Thursday, June 04, 2015	11:00 a.m. to 03:00 p.m.	Elective III/IV – Advanced Communication Theory.
Wednesday, June 10, 2015	11:00 a.m. to 02:00 p.m.	Process Instrumentation and Controller Design.

NOTE: **The candidates appearing for the examination should report 15 minutes before the start of examination.**
Mobile phones and other elctronic gazets are prohibited in the examination hall.
Change if any, in the time table shall be communicated on the university web site.

Mumbai - 400 098
30th March, 2015.

(DINESH BHONDE)
Controller of Examinations.

Ref.No:- MU/Exam/Result/FH/TT/TECH/687/328.